Tutorial 4 - SS2021
Communication Systems and Protocols

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Task 1: Serial Interface

In the figure 1.1 the pulse diagram of a RS232 interface is given. Different transmission frames have been used for the communication. A transmission frame is composed of a start bit ('0'), 5-8 data bits, no (N, none) or one bit for even (E, even) or odd (O, odd) parity, as well as at least 1 or 2 stop bits (‚1'). Possible frame formats are [5..8][N,O,E][1,2], for example 8N1 for 8 data bits, no parity bit and at least 1 stop bit.

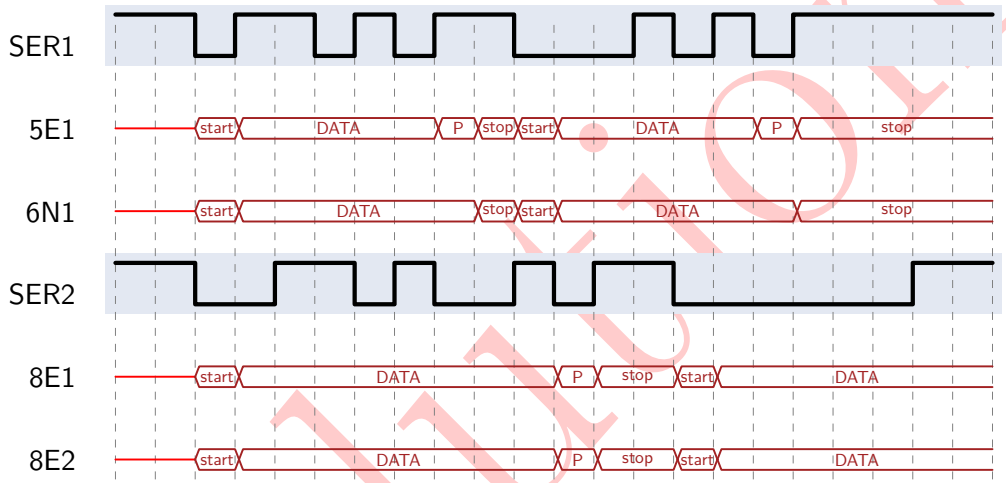

Figure 1.1: Serial interface pulse diagram

A) Give all possible frame formats for the pulse sequences as shown in figure 1.1. All given pulse sequences are describing a correct transmission. Start of a transmission is always the startbit in the third timestep. 4

For SER1, 5E1 and 6N1 are possible frame formats as both meet the requirements.
For SER2, since it is not mentioned if the Sender is sending continously or not, there are multiple frame formats possible as well.
For SER2, 8E1 and 8E2 are both possible.
8E1 allows atleast one end bit and 8E2 allows atleast 2 end bits, and both are meeting the requirements here.

B) In the figure below different pulse sequences for a RS232 interface are given. Derive from the figure and the given frame formats if the transmission was error free. Mark the erroneous parts in the pulse diagrams. 2

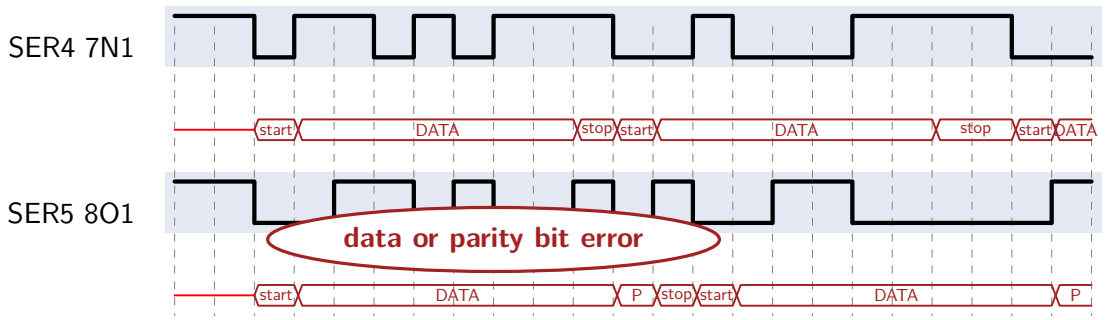

Figure 1.2: RS232 pulse sequences

C) Is it possible to detect errors without knowing the frame formats? 1

c) Not in general. The frame format gives the position and meaning of a parity bit for example.

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Task 2: Flow-Control

A communication system is given in Figure 2.1. The sender's clock frequency is 1 MHz, the receiver's is 200 kHz. Both partners work synchronously to their own clock signal and try their best to communicate as fast as possible. They apply a Level-triggered Closed-loop Flow Control corresponding to Figure 3.1 for the high-level synchronization.

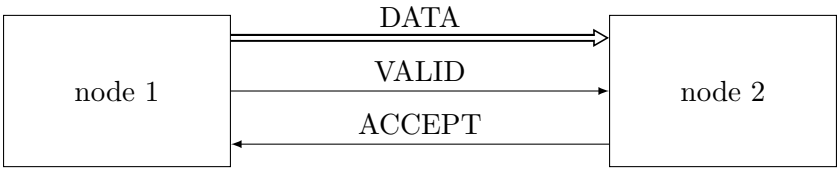

Figure 2.1: Level-triggered Closed-loop Flow Control

A) In Figure 2.2 the sensitive clock edges of the sender and the receiver as well as the signal values for the first sender clock period are shown. In order to avoid violations of setup and hold times, the data is put onto the bus and one clock cycle later the valid signal is set to '1' by the sender. The receiver will also set the accept signal one clock cycle after having received the data. Fill in the progression of all signal lines until the end of the time scale.

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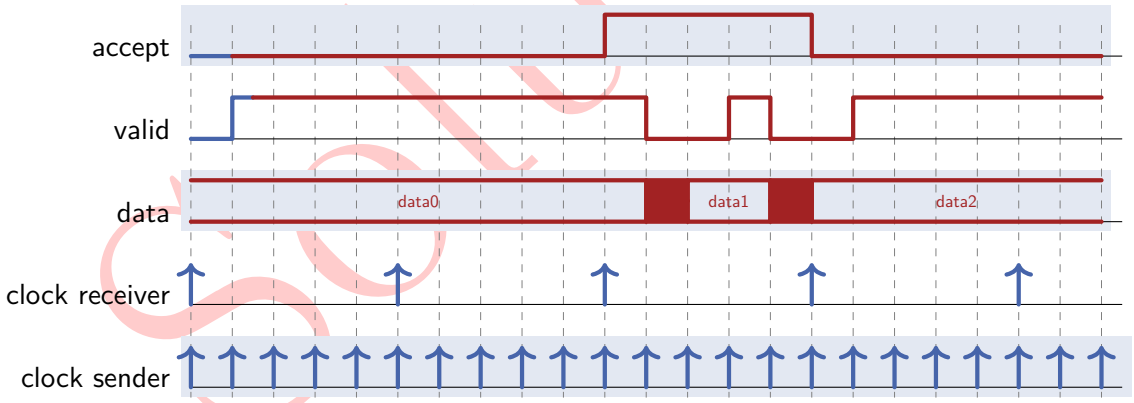

Figure 2.2: Signal progression diagram

B) Is this kind of synchronization free from error in this specific case? Justify your answer.

1

No. One can see that data1 got lost because it was put on to the data lines and removed by sender while receiver is still busy processing data0.

Recognize that data1 is lost +0.5P
Correct reasoning for the data lost +0.5P

C) Propose a better solution for this communication scenario.

1

1. Clock divider in sender so that both are only clocked at 200 kHz
2. Apply an Edge-triggered Closed-loop Flow Control
3. Clock down the sender: to avoid this loss of data, the following equation must be satisfied: $T_r \leq 4T_s$

Recognize that data1 is lost +0.5P
Correct reasoning for the data lost +0.5P

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Task 3: Cyclic Redundancy Check

Task 3.1: Transmission

To protect a data transmission, CRC with the generator polynomial $g(x) = x^2 + 1$ is used.

A) Determine the bit string that is associated with the generator polynomial. 1

Polynomial Generator: $1 \cdot x^2 + 0 \cdot x^1 + 1 \cdot x^0 \rightarrow$ Bitstring: 1 0 1

B) What is the length of the checksum that is to be appended to the data stream? 1

Length of the checksum = Order of polynomial generator. here: order $g(x) = 2$

C) Calculate the data stream that will be transmitted if the following bit string is to be protected: 1001010101. 2

Division where
Divisor : 101
Dividend : 100101010100

Computation is provided below. If the leftmost bit is '1', use divisor '101'. When the leftmost bit is '0', instead of using divisor '000' , the next bit of the dividened is pulled down.

```
  1  0  1:  1  0  0  1  0  1  0  1  0  1  0  0
          ---------------------------------------
          1  0  1
          0  0  1  1  0
             1  0  1
             0  1  1  1
                1  0  1
                0  1  0  0
                   1  0  1
                   0  0  1  1  0
                            1  0  1
                            0  1  1  1
                               1  0  1
                               0  1  0  0
                                  1  0  1
                                  0  0  1  0   Remainder
```

Bit string to be transmitted: 1001010101 10

Task 3.2: Reception

In a transmission system that uses CRC for error protection, a sender transmits the following bit stream: 100101010110. Due to interferences during transmission the last 4 bits of the bit stream are flipped before reaching the receiving node.

A) Denote the bit stream as it arrives at the receiving node. **1**

Received bit stream: 100101011001

B) Carry out the CRC error detection scheme of the receiver assuming that the generator polynomial $g(x) = x2 + 1$ has been used. **2**
What does the receiver conclude from the result? Explain and discuss the reasons for the receiver's conclusion.

Division where
Divisor : 101
Dividend : 100101011001

```
  1  0  1:  1  0  0  1  0  1  0  1  1  0  0  1
            1  0  1
            0  0  1  1  0
               1  0  1
               0  1  1  1
                  1  0  1
                  0  1  0  0
                     1  0  1
                     0  0  1  1  1
                           1  0  1
                           0  1  0  0
                              1  0  1
                              0  0  1  0  1
                                 1  0  1
                                 0  0  0   Remainder
```

Generator polynomial is too short to detect a burst error of length 4.

Task 3.3: Hardware implementation

A) To protect data transmissions in a mobile device, the CRC scheme is to be implemented using linear feedback registers with XOR operations. Draw the simplified hardware layout for the polynomial CRC-12 ($x^{12} + x^{11} + x^3 + x^2 + x + 1$). **1**